Form PTO 1449 (Rev. 2-32) U.S. Department of Commerce Patent and Trademark Office	Atty. Docket No. HEUR-016	Serial No. 10/055,088
Information Disclosure Statement by Applicant	Applicant: Arman Sagatelian et al.	
(Use several sheets if necessary)	Filed: January 22, 2002 Group: 2858	

U.S. Patent Documents

Init.		Document No.	Date	Name	Class	Subclass	Filing Date
cb	1	5,475,695	12/12/1995	Caywood et al.	371	27	03/19/1993

Foreign Documents

Init.		Document No.	Date	Country	Class	Subclass	Translation Yes	Translation No

Other Documents (Including Author, Title, Date, Pertinent Pages, etc.)

cb	2	K. Tobin, "Automated Analysis for Rapid Defect Sourcing and Yield Learning", Future Fab International, 15 pages, Vol. 4, 1997 (no month).
cb	3	"Semiconductor Spatial Signature Analysis (SSA)", [Internet] http://www-ismv.ic.ornl.gov/projects/SSA.html, 6 pages, Revised March 31, 1999, printed 2/27/03
cb	4	J. Segal et al., "The Value of Electrical Bitmap Results from Embedded Memory Arrays for Rapid Yield Learning", Digest of Papers, 2nd IEEE Latin American Test Workshop LATW2001, pp. 266-272, Feb. 2001.

Examiner: CBurtt	Date Considered: 8-20-04

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